REMARKS

Claims 2, 16, 26 and 29 have been canceled. Thus, claims 1, 3-15, 17-25, 27-28, 30-36 are now pending in the application.

Claims 5-10, 15-21, 26-28, 30 and 34-36 were objected to as being dependent on a rejected base claim. Applicant thanks the Examiner for the indication of allowable subject matter.

Claims 1-4, 11-14, 22-25, 29 and 31-33 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata in view of Khellah.

Applicant has amended independent claim 1 to include the limitations of dependent claim 2 (now canceled). Amended claim 1 is believed to distinguish over the cited prior art because that art fails to teach or suggest an operation where the source terminals of both p-channel transistors in the memory cell are applied with a first reference voltage level during the normal mode of operation, and applied with a first voltage less than the first reference voltage level during a data corruption mode of operation wherein data stored in the one or more memory cells is corrupted. Sakata teaches applying the lower voltage to just a single one of the p-channel transistors while retaining the other p-channel at a high voltage. Khellah teaches applying the same lower voltage to both p-channel transistors, but that operation occurs only during power management and most specifically the teaching is that the stored data during power management is not corrupted in this mode. Claim 1 and 11-13 are accordingly submitted as being in condition for favorable action and allowance.

Applicant has rewritten claim 3 in independent format. Rewritten claim 3 is believed to distinguish over the cited prior art because that art fails to teach or suggest an operation where

the source terminals of the first p-channel and first n-channel transistors in the memory cell are applied with a first and second reference voltage level, respectively, during the normal mode of operation, and applied with a first voltage less than the first reference voltage level and second voltage greater than the second reference voltage, respectively, during a data corruption mode of operation wherein data stored in the one or more memory cells is corrupted. Sakata teaches one embodiment which applies the lower voltage to a single one of the p-channel transistors while keeping the sources of the n-channels fixed in voltage. In another embodiment, Sakata teaches applying the higher voltage to a single one of the n-channel transistors while keeping the sources of the p-channels fixed in voltage. There is no teaching or suggestion in Sakata for combined voltage control, as claimed, being exercised over the source terminals for both the p-channel transistor (lower voltage) and n-channel transistor (higher voltage) of the memory cell for the purpose of supporting a data corruption mode of operation. Khellah does not help as it teaches applying the same lower voltage to both p-channel transistors, but that operation occurs only during power management and most specifically the teaching is that the stored data is not corrupted in this mode. Claims 3-10 are accordingly submitted as being in condition for favorable action and allowance.

Claim 14 has been amended to include the limitations of dependent claim 16 (now canceled). Applicant respectfully submits that neither cited prior art reference teaches the claimed invention where a first power supply node of a memory cell changes from a first reference voltage level to a first voltage less than the first reference voltage level and a second power supply node of that cell changes from a second reference voltage level to a second voltage greater than the second reference voltage level so as to corrupt data values stored in the memory

cell. Claims 14-15 and 17-22 are accordingly submitted as being in condition for favorable action and allowance.

Claim 23 has been amended to recite power control circuitry that places a first reference voltage on the first power supply node and a second reference voltage on the second power supply node during a normal mode of operation, and causes a first voltage less than the first reference voltage to appear on the first power supply node and a second voltage greater than the second reference voltage to appear on the second power supply node during a data corruption mode of operation. The cited prior art fails to teach a power control circuit for controlling the first and second power supply nodes in this manner. Claims 23-24 are accordingly submitted as being in condition for favorable action and allowance.

Claim 25 has been amended to include nearly all of the limitations of original claim 23 as well as the limitations of claim 29 (now canceled). Amended claim 25 is believed to be patentable over the cited prior art because that art fails to teach or suggest power control circuitry that places a first reference voltage on the first power supply node (coupled to the sources of both p-channel transistors) and a second reference voltage on the second power supply node during a normal mode of operation, and causing a first voltage less than the first reference voltage to appear on the first power supply node (and thus on the sources of the two p-channel transistors) during a data corruption mode of operation wherein the one or more data values stored in each of the one or more memory cells are corrupted. Claims 25 and 27-28 are accordingly submitted as being in condition for favorable action and allowance.

Claim 30 has been amended to include the limitations of claims 23 and 25 as well as limitations relating to the application of a second voltage greater than the second reference

voltage on the second power supply node during a data corruption mode of operation. This operation of the power control circuitry as to the first and second power supply nodes is neither disclosed nor suggested by the cited prior art. Accordingly, Applicant submits that claims 30-36 are in condition for favorable action and allowance.

Respectfully submitted,
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